

# Investigating Surface Loss Effects in Superconducting Transmon Qubits

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**Abstract**—Superconducting qubits are sensitive to a variety of loss mechanisms including dielectric loss from interfaces. By changing the physical footprint of the qubit, it is possible to modulate sensitivity to surface loss. Here, we show a systematic study of planar superconducting transmons of differing physical footprints to optimize the qubit design for maximum coherence. We find that qubits with small footprints are limited by surface loss and that qubits with large footprints are limited by other loss mechanisms, which are currently not understood.

**Index Terms**—Dielectric loss, quantum noise, superconducting qubits.

## I. INTRODUCTION

IMPROVING coherence times (or quality factors) of superconducting qubits is necessary in order to implement meaningful tests of quantum information processing in such systems. It has been known for many years that dielectric loss can play a potentially limiting role for qubit coherence [1]. While other loss mechanisms such as quasi-particle loss [2], [3], limitations due to infrared (*IR*) radiation [4], [5], losses related to the qubit readout [6], or electromagnetic radiation [7] can play dominant roles, a picture has been emerging recently that dielectric loss at surfaces also plays a key role [8]–[11]. In particular, it has been observed that quality factors tend to increase when the physical footprint of the devices increases for resonators [9], [10], two-dimensional (2-D) transmon qubits [12], and 3-D qubits [13], [14]. This points to surface loss as a detractor of qubit coherence, suggesting that qubits can be optimized for coherence by increasing the physical footprint. However, simply continuing to increase physical size is not a guarantee for further improvements in coherence times as other loss mechanisms can become dominant. It is therefore important to design qubits that are sensitive to specific loss mechanisms and perform a systematic study to optimize qubit coherence times.

Inspired by similar work for 3-D qubits [14], we here implement a study for the 2-D transmon qubits [15] fabricated

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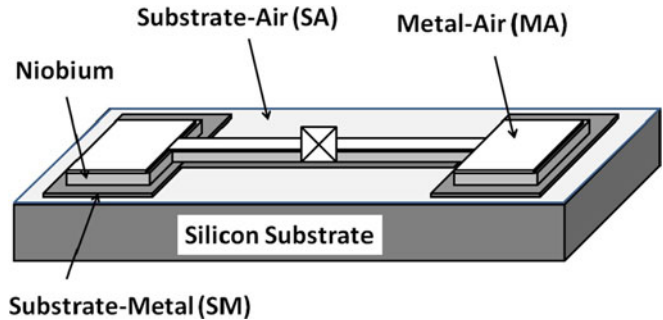


Fig. 1. Schematic of a superconducting qubit fabricated on top of a silicon substrate. Surface loss can arise due to the contributions from the SA interface, the SM interface, and the MA interface.

on high-resistivity silicon. Anticipating energy dissipation from surface loss, we tested several styles of transmon qubits. From these studies, we find that the qubits with physically small shunting capacitors (i.e., a small physical footprint) show a characteristic  $T_1$  decay that is likely limited by losses associated with one or more surfaces (see Fig. 1) though the present data are not sufficient to pinpoint which surface dominates. Meanwhile qubits with physically large footprints show a characteristic  $T_1$  that appears to be limited by contributions of currently unknown origin and saturates near  $T_1 \sim 50 \mu\text{s}$ , corresponding to a quality factor  $Q = T_1 2\pi f \sim 1.5 \text{ M}$ , where  $f \sim 4\text{--}5 \text{ GHz}$  is the qubit frequency.

All presented  $T_1$  times are typically averaged over several hours and in most cases fluctuations on the order of  $\pm 20\%$  have been observed, although fluctuations by as much as a factor of 2–4 $\times$  have been noticed in some of the rare cases. We believe these are real  $T_1$  fluctuations because the uncertainty from each fit is typically less than the measured  $T_1$  variations with time. Since  $T_1$  itself appears to be fluctuating, the values that are shown should be interpreted with a sizable error bar. We believe that in the long term it is useful to introduce metrics to quantify these fluctuations so that experiments or improvements can be more readily compared. Despite these fluctuations, meaningful information can be extracted from our experiments described below.

## II. DESIGN AND SIMULATION

A systematic study of coherence times as a function of qubit geometry has been done for the 3-D transmon qubits on sapphire [14], and we adopt similar strategies here. The experimental goal

TABLE I  
SUMMARY OF SIMULATED SURFACE PARTICIPATION TO QUBIT LOSS FOR THE FIVE DIFFERENT QUBIT DESIGNS WITH A SUBSTRATE TRENCH DEPTH OF 50 NM

	MOD A	MOD B	MOD C	MOD D	MOD E
SM	$3.68 \times 10^6$	$1.10 \times 10^6$	$3.46 \times 10^5$	$2.15 \times 10^5$	$1.20 \times 10^5$
SA	$1.24 \times 10^6$	$3.32 \times 10^5$	$9.10 \times 10^4$	$5.04 \times 10^4$	$2.38 \times 10^4$
MA	$7.20 \times 10^4$	$1.62 \times 10^4$	$3.80 \times 10^3$	$1.80 \times 10^3$	$6.0 \times 10^2$

Of particular interest is the significant change in SA participation between MOD A and B. It is also interesting to note that the MA participation is simulated to be very small.

is to design, fabricate, and test transmon qubits with identical anharmonicities of approximately  $E_c \sim 350$  MHz but substantially different physical sizes for the shunting capacitor to test how  $T_1$  times vary and compare the results to theory.

A total of five qubit styles were designed and simulated using Ansys HFSS and Q3D software, and shown in Figs. 4–8. We refer to these different designs as MOD A through MOD E. Participation factors were determined by calculating the corresponding energy based on the electric fields present at particular surfaces and interfaces within the build. Hypothetical layers possessing a dielectric constant of  $\epsilon_r = 5$  [14] were placed between the substrate and overlying metallization (SM), which includes the capacitors, groundplane, and adjacent readout resonator, the top surface of the substrate exposed to air (SA), and the metallization surfaces exposed to air (MA). Continuous layers of uniform thickness were assumed, but because the thickness of these layers was not known *a priori*, the units of the calculated surface participation factors in Table I are  $\text{m}^{-1}$ . For a given layer, multiplying the participation factor by the thickness and  $\tan(\delta)$  gives the reciprocal of the qubit quality factor  $Q$  assuming no other sources of loss.

Because the thicknesses of these contamination layers are presumed to be much thinner ( $< 10$  nm) than the dimensions of the constitutive elements of the qubit metallization, the constraints on the domain discretization necessary to produce a credible numerical solution made conventional simulation impractical. Instead we adopted a strategy of calculating the effective electric field strength at a specific interface by first assuming no contamination layer and extrapolating the solution to a different dielectric constant than those on either side of the original interface [14]. The effective fields were calculated by matching the appropriate components of the electric fields as prescribed by the boundary conditions between two dielectric layers

$$\vec{E}_{\parallel}^{(1)} = \vec{E}_{\parallel}^{(2)} \quad (1)$$

$$\epsilon_1 \vec{E}_{\perp}^{(1)} = \epsilon_2 \vec{E}_{\perp}^{(2)} \quad (2)$$

where  $\vec{E}_{\parallel} = -(\vec{E} \times \vec{n}) \times \vec{n}$  is the component of the field parallel to the interface,  $\vec{E}_{\perp} = \vec{n}(\vec{E} \cdot \vec{n})$  is that normal to the interface, superscript 1 refers to the hypothetical contamination layer, and 2 the actual dielectric material present in the simulation (e.g., silicon for the substrate surfaces or vacuum for the free surfaces). Combining (1) and (2), we arrive at the effective electric

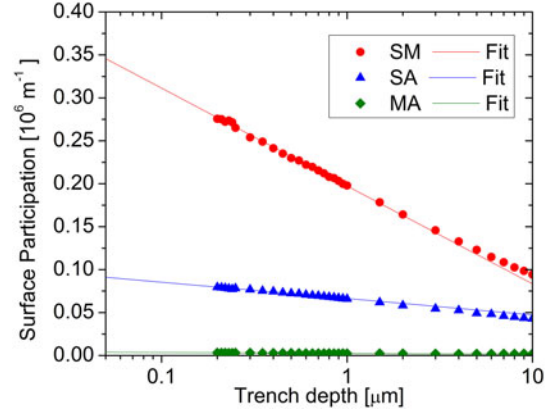


Fig. 2. Calculated surface participation factors for the SM, SA, and MA interfaces as a function of qubit pocket trench depth for the MOD C qubit design. The participation factors obey a logarithmic dependence for small trench depths ( $< 1 \mu\text{m}$ ), which is predicted by the  $r^{-\frac{1}{2}}$  electric field dependence near the metallization edges. Below trench depths of 300 nm, surface participation factors were extrapolated using the logarithmic fits (solid lines) due to the simulation convergence issues arising from the singular behavior of the electric fields.

field in the contamination layer with dielectric constant  $\epsilon_1$

$$\vec{E}^{(1)} = \frac{\epsilon_2}{\epsilon_1} \vec{n}(\vec{E}^{(2)} \cdot \vec{n}) - (\vec{E}^{(2)} \times \vec{n}) \times \vec{n}. \quad (3)$$

Calculations of the surface participation factors  $p_i/t_i$  were then conducted by assuming a uniform electric field strength throughout the layer thickness  $t_i$  and integrating over the corresponding surface  $S$

$$\frac{p_i}{t_i} \approx \frac{\int_S \vec{E}^{(1)} \cdot \epsilon_1 \vec{E}^{*(1)} dS}{U_{\text{tot}}} \quad (4)$$

where  $\vec{E}^*$  is the conjugate of  $\vec{E}$  and  $U_{\text{tot}}$  is the total energy of the system.

Additional complications are that the electric field diverges near corners, and that the etching procedures used in the fabrication of the 2-D transmon qubits result in some degree of recess of the substrate surface in the qubit pocket. It is thus important to incorporate the effects of trenching in the surface participation calculations. HFSS models were generated that included both 200-nm-thick niobium (Nb) metallization and a variation in the pocket trench depth. Identical qubit junctions, treated as lumped elements, were used for all of the MOD's under investigation. Because the singular nature of the electric fields near the edges of the Nb metallization can lead to convergence issues in the simulations of trench depths less than  $\sim 200$ – $300$  nm, we restricted the modeling to trenches greater than this thickness and extrapolated participation factors of the various interfaces according to a logarithmic fit with respect to the trench depth. Because the electric field strength obeys a  $r^{-\frac{1}{2}}$  dependence for a thin metallic sheet [16], where  $r$  is the distance from the sheet edge, the integrand in (4) should scale as  $r^{-1}$  for small  $r$  and a corresponding  $\log(r)$  scaling of the surface participation. Although simulations based on the finite element method may be susceptible to errors due to the presence of these singularities, the logarithmic dependence in surface participation observed in Fig. 2 suggests that their contributions to the electric field

energy are being sufficiently captured. Table I contains the extrapolated participation factors to a trench depth of 50 nm for all of the designs, demonstrating that the substrate–metal (SM) interface participation varies by a factor of  $30\times$  over the different designs, the substrate–air (SA) interface participation varies about a factor of  $50\times$ , and while the metal–air (MA) interface participation varies over two orders of magnitude, its participation is substantially less than that of the SM and SA interfaces and is likely not contributing to the loss.

Substrate participation was simulated using HFSS in a similar manner as that used for the surface participation factors. The substrate participation asymptotes to a constant value in the limit that the trench depth approaches zero. In this limit, in which the magnitude of the electric fields present in the dielectric substrate and in vacuum ( $\epsilon_r = 1$ ) are equal, the substrate participation approaches  $\frac{\epsilon_{\text{sub}}}{\epsilon_{\text{sub}} + 1} = 0.92$  for all of the MOD's. Here and in all simulations, we have assumed the dielectric constant of the substrate as  $\epsilon_{\text{sub}} = 11.45$ .

Chip sizes were  $4 \times 7$  and  $4 \times 8$  mm<sup>2</sup>, small enough that the fundamental chip mode was located above 10 GHz. Each chip consists of a single  $50 \Omega$  feedline, out of which four  $\lambda/2$  coplanar waveguide (CPW) resonators (also  $50 \Omega$ ) are each terminated by a transmon qubit of identical design. The resonator frequencies are staggered at 6.75, 7.0, 7.25, 7.5 GHz with a coupling quality factor of 10 000–40 000. Given qubit-resonator coupling strengths in the range of  $g = 10$ –50 MHz, we calculate the Purcell loss [17] to be negligible in all our experiments with qubit frequencies targeted in the  $f = 4$ –5 GHz range. The qubit chip is back mounted to a printed circuit (PC) board and placed in a light tight enclosure to minimize the exposure to *IR* radiation [4], [5]. Most  $T_1$  measurements were done using the high-power readout [6]. To ensure no residual effects from the readout are present [3], we varied the repetition time or employed standard low-power quantum non-demolition (QND) measurements for many samples (but not all) and observed no noticeable differences. The input attenuation and filtering to the sample varied slightly between experiments to test thermal dephasing [18], but these variations were found to have little impact, if any, on  $T_1$  times. However, because  $T_2$  times are typically near  $T_1$ , there is still room for improvement for future experiments. The output lines included PAMTECH 3–12 GHz isolators (model CWJ0312KI) and a 4K HEMT amplifier by CalTech.

### III. FABRICATION, TESTING, AND RESULTS

The qubits were fabricated on high-resistivity ( $\rho \sim 1$  k $\Omega$ cm) silicon, which received a hydrogen fluoride (HF) clean just prior to the metallization. Approximately 200 nm of Nb was physical vapor deposited at a rate of 1.7 nm/s. The junctions were fabricated using a cold develop and acetone lift off at room temperature. Each wafer received a Huang clean (also known as an radio corporation of america (RCA) clean [19]) to remove organic and inorganic contaminants from the wafer surface. Within 30 min prior to the 200-nm Nb deposition, each wafer received a 2 min 100:1 HF clean to remove the surface SiO<sub>x</sub>. After the HF treatment, each wafer received a 5 min water rinse. After the water rinse and dry, a thin SiO<sub>x</sub> layer remained

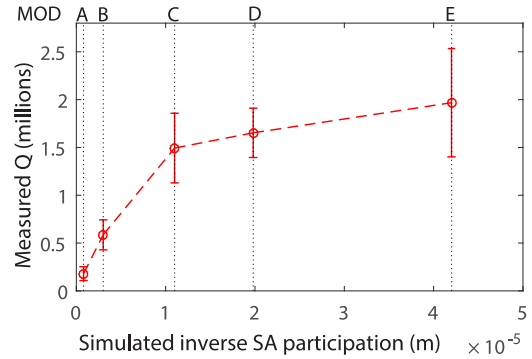


Fig. 3. Qubit quality factor as a function of the inverse SA surface participation. Markers indicate the average, and error bars indicate  $\pm$  the standard deviation divided by the square root of the number of measured qubits. The data indicate that low MOD qubits are consistent with surface loss due to linear scaling with the simulation. Coherence of high-MOD qubits appears to be much less sensitive to surface loss, seemingly limited by another loss mechanism.

on the surface. Next, a chlorine-based reactive ion etch (RIE) etch was performed, which slightly overetches the silicon, etching approximately 50–100 nm into the silicon. The aluminum–aluminum oxide–aluminum Josephson junction was fabricated using a Dolan bridge [20] employing polymethyl methacrylate / methyl methacrylate (PMMA/MMA) processing steps. The aluminum makes contact to the Nb after applying a gentle low-power ion mill clean prior to the aluminum deposition. We have tested additional qubits (data not shown) with slight modifications to the precleans prior to the Nb deposition, but found no deviations from the data reported here, and similarly a junction liftoff in microposit remover 1165 at 80 °C was also found not to affect coherence times.

The measured  $T_1$  times are translated into quality factors in order to remove effects from frequency variations of the qubits; within the range of qubit frequencies measured, no frequency dependence of the quality factor was found. The results are summarized in Fig. 3, where the measured quality factors are plotted against the inverse of simulated SA surface loss participation values. If coherence times were limited by SA loss, we would expect  $Q$  to linearly scale with the inverse of the participation values. Each data point represents the mean quality factor of eight qubits, and the error bar is the standard deviation divided by the square root of the number of measured qubits. Each  $T_1$  is obtained by averaging typically on the order of a few hours to account for known fluctuations. We observe a dramatic improvement in  $Q$  between MOD A and MOD B qubits, consistent with predictions based on the surface loss. When plotted against SM or MA inverse surface participation values (not shown), the results look very similar, which leads us to the conclusion that at present, the data are not sufficient to ascertain which of the interfaces dominates. High-MOD qubits appear to saturate near  $Q \sim 1.5$ –2 M indicating a loss contribution of unknown origin, which could potentially include substrate loss, loss due to quasi-particles [3], residual coupling to resistive metallic components housing the qubits, or other mechanisms. Nonetheless, it is possible to place an upper bound on the bulk loss of the silicon

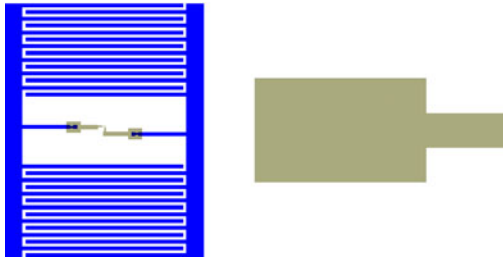


Fig. 4. Schematic of the MOD A design featuring an interdigitated capacitor with a finger linewidth and finger-to-finger spacing of  $1 \mu\text{m}$ . The rectangle to the right is the coupling capacitor to the CPW readout resonator of sufficient size such that  $g = 8 \text{ MHz}$ .

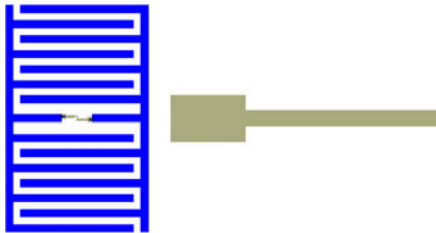


Fig. 5. Schematic of the MOD B design featuring an interdigitated capacitor with a finger linewidth and finger-to-finger spacing of  $5 \mu\text{m}$ . The rectangle to the right is the coupling capacitor to the CPW readout resonator of sufficient size such that  $g = 20 \text{ MHz}$ .

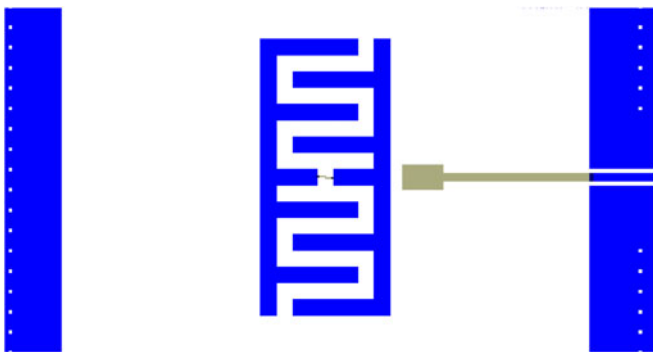


Fig. 6. Schematic of the MOD C design featuring an interdigitated capacitor with a finger linewidth and finger-to-finger spacing of  $20 \mu\text{m}$ . The rectangle to the right is the coupling capacitor to the CPW readout resonator of sufficient size such that  $g = 45 \text{ MHz}$ .

of  $\tan(\delta) \sim 5 \times 10^{-7}$ , though we believe the actual number is likely less.

#### IV. PICTURES OF THE QUBIT DESIGNS

Figs. 4–8 depict each of the five MOD designs in detail. Note that all qubits are placed inside a grounding box of dimension  $650 \times 650 \mu\text{m}^2$ . This box is only fully visible for MODs D and E. MODs A and B were also tested with a larger coupling capacitor to increase the signal-to-noise ratio. The data indicate no appreciable effect on  $T_1$ , which is not surprising given that the calculated Purcell limit is much larger than the observed coherence times.

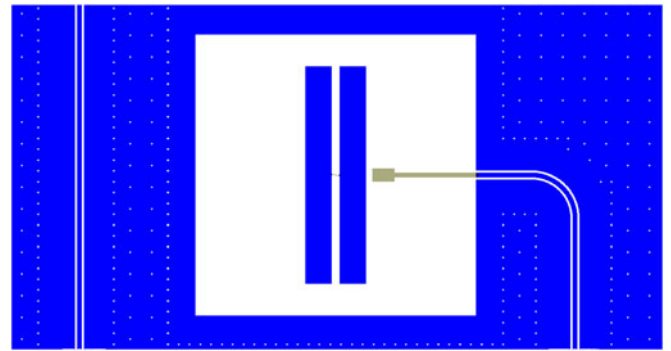


Fig. 7. Schematic of the MOD D design featuring two capacitor pads of dimension  $500 \times 60 \mu\text{m}^2$  separated by  $20 \mu\text{m}$ . The rectangle to the right is the coupling capacitor to the CPW readout resonator of sufficient size such that  $g = 52 \text{ MHz}$ .

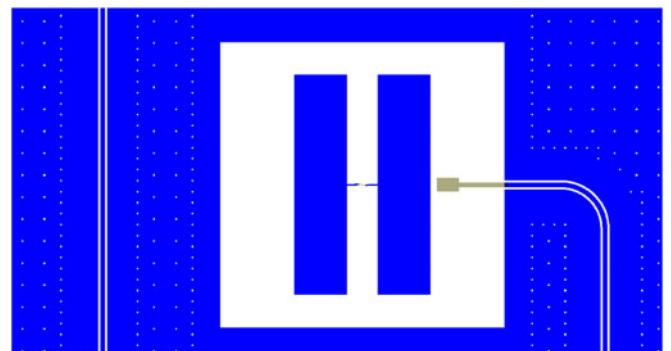


Fig. 8. Schematic of the MOD E design featuring two capacitor pads of dimension  $500 \times 120 \mu\text{m}^2$  separated by  $70 \mu\text{m}$ . The rectangle to the right is the coupling capacitor to the CPW readout resonator of sufficient size such that  $g = 53 \text{ MHz}$ .

#### V. CONCLUSION

In conclusion, we present a systematic study of quality factors in qubits with widely varying degrees of surface participation. Results indicate that depending on the design, qubits can be either limited by surface loss (low-MOD qubits) or an additional loss mechanism (high-MOD qubits) that is currently not well understood. The experimental results are not sufficient for us to make any claims on which surface dominates surface loss. We believe the methods applied here should allow for optimal design of qubits for long coherence to enable relevant multiqubit implementations. The results also motivate the development of cleaning methods to potentially enable smaller footprint qubits with good coherence in the future, as well as the development of additional strategies to understand new loss mechanisms for high-MOD qubits.

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